

The 2652 Multi-Protocol Communications Controller (MPCC) is a monolithic n-channel MOS LSI circuit that formats, transmits and receives synchronous serial data while supporting bit-oriented or byte control protocols. The chip is TTL compatible, operates from a single +5V supply, and can interface to a processor with an 8 or 16-bit bidirectional data bus.

- DC to 500K bps data rate
- Protocol management
 - Bit-oriented protocols (BOP): SDLC, ADCCP, HDLC
 - Byte-control protocols (BCP): BI-SYNC, DDCMP
- Programmable operation
 - 8 or 16-bit tri-state data bus
 - Protocol selection—BOP or BCP
 - Error control—CRC or VRC or no error check
 - Character length—1 to 8 bits for BOP or 5 to 8 bits for BCP
 - SYNC or secondary station address comparison for BCP-BOP
 - Idle transmission of SYNC/FLAG or MARK for BCP-BOP

- Automatic detection and generation of special BOP control sequences, i.e., FLAG, ABORT, GA
- Zero insertion and deletion for BOP
- Short character detection for last BOP data character
- SYNC generation, detection, and stripping for BCP
- Maintenance Mode for self-testing
- Common parameter control registers
- Independent status and data registers for receive and transmit
- Status indicator signals can be used as CPU interrupts
- TTL compatible
- 40-pin package
- Single +5V supply

- Intelligent terminals
- Line controllers
- Network processors
- Front end communications
- Remote data concentrators
- Communication test equipment
- Computer to computer links

IWA PACKAGE			
CE	1	40	MM
RxC	2	39	TxC
RxSI	3	38	TxSQ
S/F	4	37	TxE
TxA	5	36	TxU
RxDA	6	35	TxBE
RxSA	7	34	TxA
RxE	8	33	RESET
GND	9	32	VCC
DB08	10	31	DB00
DB09	11	30	DB01
DB10	12	29	DB02
DB11	13	28	DB03
DB12	14	27	DB04
DB13	15	26	DB05
DB14	16	25	DB06
DB15	17	24	DB07
R/W	18	23	OBEN
A2	19	22	BYTE
A1	20	21	A0

NOTE

00 is least significant bit, highest number (that is, DB15, A2) is most significant bit.

The block diagram illustrates the internal architecture of the 68010 microprocessor. A central vertical bar represents the **INTERNAL BUS**. Key components and their connections are as follows:

- DATA BUS BUFFER:** Connected to the external **DB15-DB00** bus and the internal bus.
- RESET and MM:** External control signals connected to the internal bus.
- READ/ WRITE LOGIC AND CONTROL:** Receives external signals **A2-A0**, **BYTE**, **R/W**, **CE**, and **D BEN**. It connects to the internal bus.
- PARAMETER CONTROL SYNC/ADDRESS REGISTER (PCSAAR):** A 16-bit register connected to the internal bus and the **PARAMETER CONTROL REGISTER (PCR)**.
- PARAMETER CONTROL REGISTER (PCR):** An 8-bit register connected to the PCSAAR and the **TRANSMITTER DATA/STATUS REGISTER (TDSR)**.
- RECEIVER DATA/STATUS REGISTER (RDSR):** A 16-bit register connected to the internal bus and the PCSAAR.
- TRANSMITTER DATA/STATUS REGISTER (TDSR):** A 16-bit register connected to the PCR and the **TRANSMITTER LOGIC AND CONTROL**.
- RECEIVER LOGIC AND CONTROL:** Connected to the internal bus and the RDSR. It has multiple outputs for external signals: **S/F**, **RxE**, **RxA**, **RxDA**, **RxSA**, **RxC**, and **RxSI**.
- TRANSMITTER LOGIC AND CONTROL:** Connected to the TDSR. It has multiple outputs for external signals: **TxE**, **TxA**, **TxBE**, **TxU**, **TxC**, and **TxSO**.

Power supply connections are indicated at the top right: **VCC** and **GND**.

PIN DESIGNATION

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
DB15-DB00	17-10 24-31	I/O	Data Bus: DB07-DB00 contain bidirectional data while DB15-DB08 contain control and status information to or from the processor. Corresponding bits of the high and low order bytes can be WIRE OR'ed onto an 8-bit data bus.
A2-A0	19-21	I	Address Bus: A2-A0 select internal registers. The four 16-bit registers can be addressed on a word or byte basis. See Register Address section.
BYTE	22	I	Byte: Single byte (8 bit) data bus transfers are specified when this input is high. A low level specifies 16 bit data bus transfers.
CE	1	I	Chip Enable: A high input permits a data bus operation when DBEN is activated.
$\bar{R}/\bar{W}$	18	I	Read/Write: $\bar{R}/\bar{W}$ controls the direction of data bus transfer. When high, the data is to be loaded into the addressed register. A low input causes the contents of the addressed register to be presented on the data bus.
DBEN	23	I	Data Bus Enable: After A2-A0, CE, BYTE and $\bar{R}/\bar{W}$ are set up, DBEN may be strobed. During a read, the tri-state data bus (DB) is enabled with information for the processor. During a write, the stable data is loaded into the addressed register and TxBE will be reset if TDSR was addressed.
RESET	33	I	Reset: A high level initializes all internal registers and timing.
MM	40	I	Maintenance Mode: MM internally gates TxSO back to RxSI and $\bar{T}xC$ to RxC for off line diagnostic purposes. The RxC input is disabled when MM is asserted.
RxE	8	I	Receiver Enable: A high level input permits the processing of RxSI data. A low level disables the receiver logic and initializes all receiver registers and timing.
RxA	5	O	Receiver Active: RxA is asserted when the first data character of a message is ready for the processor. In the BOP mode this character is the address. The received address must match the secondary station address if the MPCC is a secondary station. In BCP mode, if strip-SYNC (PCSAR ₁₃) is set, the first non-SYNC character is the first data character; if strip-SYNC is zero, the character following the second SYNC is the first data character. In the BOP mode, the closing FLAG resets RxA. In the BCP mode, RxA is reset by a low level at RxE.
RxDA*	6	O	Receiver Data Available: RxDA is asserted when an assembled character is in RDSRL and is ready to be presented to the processor. This output is reset when RDSRL is read.
RxC	2	I	Receiver Clock: RxC(1X) provides timing for the receiver logic. The positive going edge shifts serial data into the RxSR from RxSI.
S/F	4	O	SYNC/FLAG: S/F is asserted for one RxC clock time when a SYNC or FLAG character is detected.
RxSA*	7	O	Receiver Status Available: RxSA is asserted when there is a zero to one transition of any bit in RDSRH except for RSOM. It is cleared when RDSRH is read.
RxSI	3	I	Receiver Serial Input: RxSI is the received serial data. Mark = '1', space = '0'.
TxE	37	I	Transmitter Enable: A high level input enables the transmitter data path between TDSRL and TxS0. At the end of a message, a low level input causes TxS0 = 1 (mark) and TxA = 0 after the closing FLAG (BOP) or last character (BCP) is output on TxS0.
TxA	34	O	Transmitter Active: TxA is asserted when TxE is high and TSOM (TDSR ₀) is set. This output will reset when TxE is low and the closing FLAG (BOP) or last character (BCP) has been output on TxS0.
TxBE*	35	O	Transmitter Buffer Empty: TxBE is asserted when the TDSR is ready to be loaded with new control information or data. The processor should respond by loading the TDSR which resets TxBE.
TxU*	36	O	Transmitter Underrun: TxU is asserted during a transmit sequence when the service of TxBE has been delayed for more than one character time. This indicates the processor is not keeping up with the transmitter (TxS0 depends on PCSAR ₁₁). TxU is reset by RESET or setting of TSOM (TDSR ₀).
TxC	39	I	Transmitter Clock: TxC (1X) provides timing for the transmitter logic. The positive going edge shifts data out of the TxSR to TxS0.
TxS0	38	O	Transmitter Serial Output. TxS0 is the transmitted serial data. Mark = '1', space = '0'.
VCC	32	I	+5V: Power supply.
GND	9	I	Ground: 0V reference ground.

*Indicates possible interrupt signal.

REGISTERS		NO. OF BITS	DESCRIPTION*
Addressable	PCSAR	16	PCSAR _H and PCR contain parameters common to the receiver and transmitter. PCSAR _L contains a programmable SYNC character (BCP) or secondary station address (BOP).
	PCR	8	
	RDSR	16	RDSR _H contains receiver status information. RDSR _L = RxDB contains the received assembled character.
	TDSR	16	TDSR _H contains transmitter command and status information. TDSR _L = TxDB contains the received assembled character.
Internal	CCSR	8	These registers are used for character assembly (CCSR, HSR, RxSR), disassembly (TxSR), and CRC accumulation/generation (RxCRC, TxCRC).
	HSR	16	
	RxSR	8	
	TxSR	8	
	RxCRC	16	
	TxCRC	16	

NOTE

*H = High byte - bits 15-8

L = Low byte - bits 7-0

Table 1 GLOSSARY

CHARACTER	DESCRIPTION
FCS	Frame Check Sequence is transmitted/received as 16 bits following the last data character of a BOP message and is usually CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) with dividend preset to 1's.
BCC	Block Check Character is transmitted/received as two successive characters following the last data character of a BCP message. Either CRC-16 ($X^{16} + X^{15} + X^2 + 1$) with dividend preset to 0's or LRC ($X^8 + 1$) as computed by the processor, is polynomial. CRC-16 is used with 8-bit EBC DIC. LRC is used with 7-bit ASCII in conjunction with VRC. The CRC-16 is computed on all characters beginning with the first non-sync character at the start of the message.

Table 2 ERROR CONTROL

FUNCTIONAL DESCRIPTION

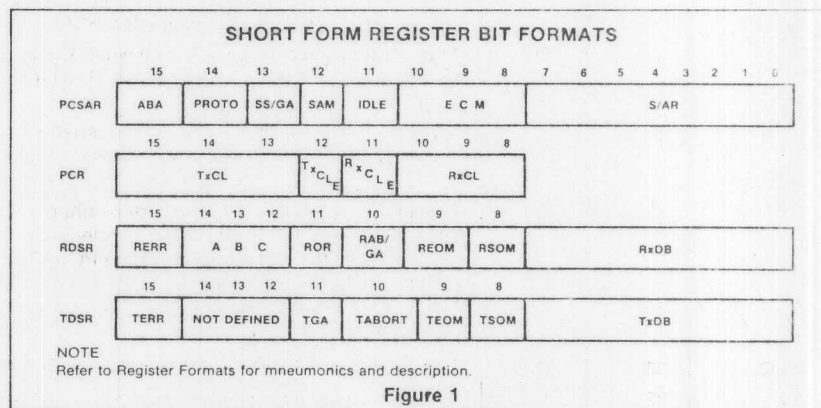
The MPCC can be functionally partitioned into receiver logic, transmitter logic, registers that can be read or loaded by the processor, and data bus control circuitry. The MPCC block diagram is shown in Figure 1 while the receiver and transmitter data paths are depicted in Figures 2 and 3.

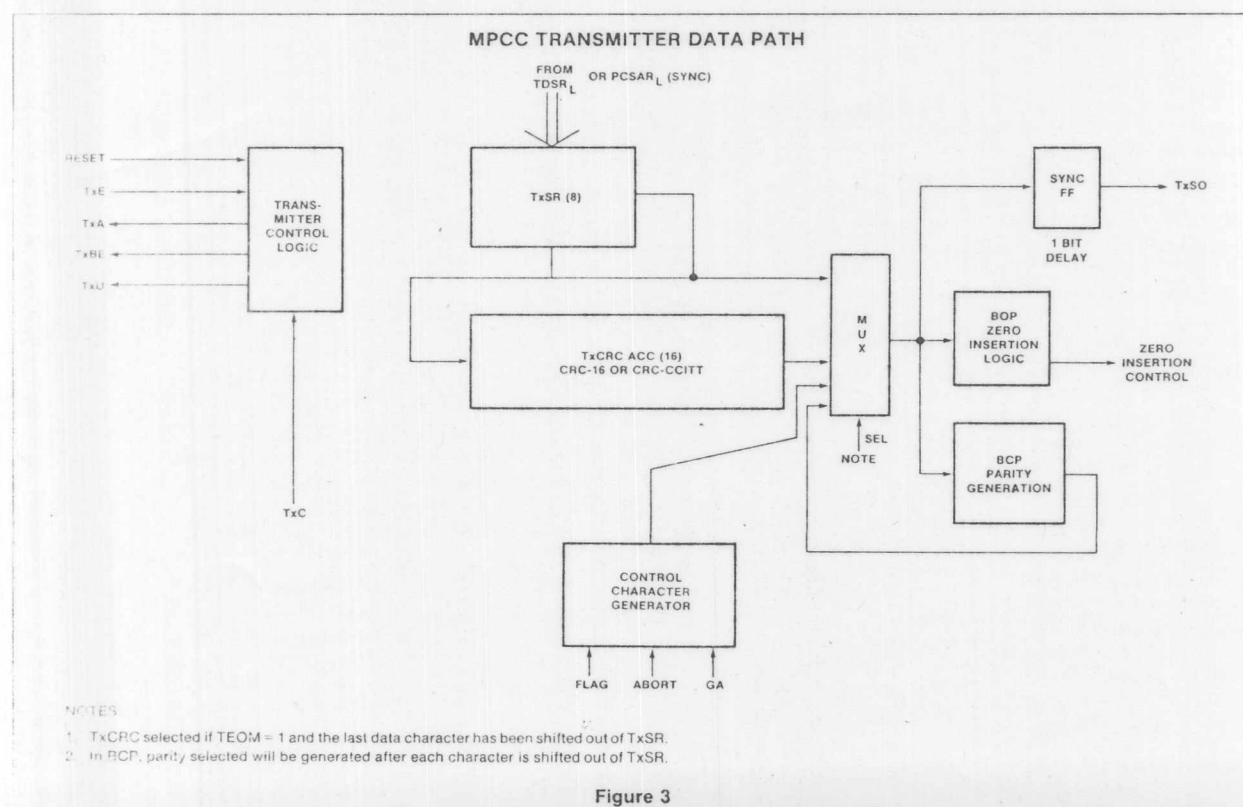
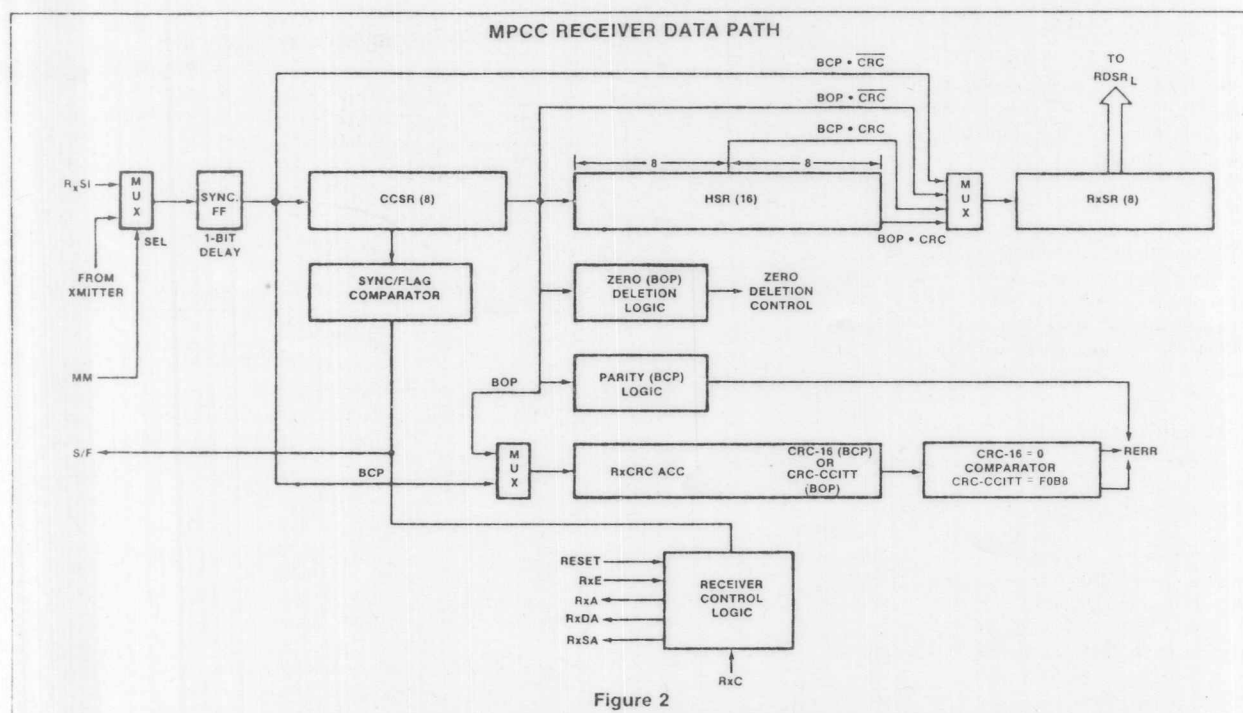
OPERATION	BIT PATTERN	FUNCTION
BOP	01111110	Frame message
FLAG	11111111 generation	Terminate communication
ABORT	01111111 detection	
GA	01111111	Terminate loop mode repeater function
Address	(PCSAR _L) ¹	Secondary station address
BCP		
SYNC	(PCSAR _L) or (TxDB) ² generation	Frame message

NOTES

1. (∞) refers to contents of ∞
2. For IDLE = 0 or 1 respectively

Table 3 SPECIAL CHARACTERS





RECEIVER OPERATION

General

After initializing the parameter control registers (PCSAAR and PCR), the RxE input must be set high to enable the receiver data path. The serial data on the RxSI is synchronized and shifted into an 8-bit Control Character Shift Register (CCSR) on the rising edge of RxC. A comparison between CCSR contents and the FLAG (BOP) or SYNC (BCP) character is made until a match is found. At that time, the S/F output is asserted for one RxC time and the 16-bit Holding Shift Register (HSR) is enabled. The receiver then operates as described below.

BOP Operation

A flow chart of receiver operation in BOP mode appears in Figure 4. Zero deletion (after five ones are received) is implemented on the received serial data so that a data character will not be interpreted as a FLAG, ABORT, or GA. Bits following the FLAG are shifted through the CCSR, HSR, and into the Receiver Shift Register (RxSR). A character will be assembled in the RxSR and transferred to the RDSR_L for presentation to the processor. At that time the RxDA output will be asserted and the processor must take the character before the next character is assembled in the RxSR. If not, an overrun (RDSR₁₁ = 1) will occur and succeeding characters will be lost.

The first character following the FLAG is the secondary station address. If the MPCC is a secondary station (PCRSAR₁₂ = 1), the contents of RxSR are compared with the address stored in PCSAR_L. A match indicates the forthcoming message is intended for the station; the RxA output is asserted, the character is loaded into RDSR_L, RxDA is asserted and the Receive Start of Message bit (RSOM) is set. No match indicates that another station is being addressed and the receiver searches for the next FLAG.

If the MPCC is receiving data from a secondary station ($PCSAR_{12} = 0$), no secondary address check is made; RxA is asserted and $RSOM$ is set once the first non-FLAG character has been loaded into $RDSR_L$ and $RxDA$ has been asserted.

When the 8 bits following the address character have been loaded into RDSRL and RxDA has been asserted, RSOM will be cleared. The processor should read this 8-bit character and interpret it as the Control field.

Received serial data that follows is read and interpreted as the Information field by the processor. It will be assembled into character lengths as specified by PCR₈₋₁₀. As

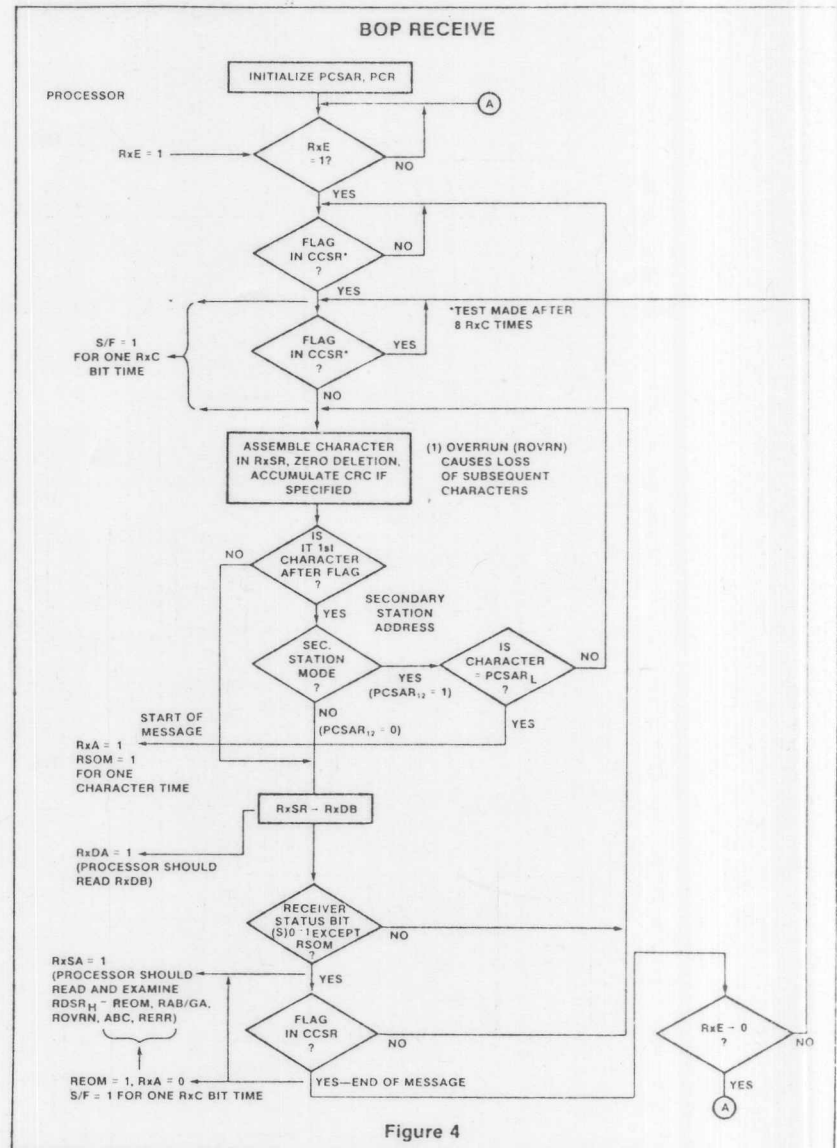


Figure 4

before, RxDA is asserted each time a character has been transferred into RDSR_L and is cleared when RDSR_L is read by the processor. RxSA is asserted when there is a zero to one transition for any bit in RDSR_H except for RSOM. RxSA and all bits in RDSR_H except RSOM are cleared when RDSR_H is read. The processor should check RDSR₉₋₁₅ each time RxSA is asserted. If RDSR₉ is set, then RDSR₁₂₋₁₅ should be examined.

Receiver character length may be changed dynamically in response to RxDA: read the character in RxDB and write the new char-

acter length into RxCL. The character length will be changed on the next RxC positive going edge.

The CRC-CCITT, if specified by PCSAR₈₋₁₀, is accumulated in RxCRC on each character following the FLAG. When the closing FLAG is detected in the CCSR, the received CRC is in the 16-bit HSR. At that time, the Receive End of Message bit (REOM) will be set; RxSA and RxDA will be asserted. The processor should read the last data character in RDSR_L and the receiver status in RDSR₉₋₁₅. If RDSR₁₅ = 1, there has been a

transmission error; the accumulated CRC-CCITT is incorrect. If $RDSR_{12-14} \neq 0$, the last data character is not of prescribed length. Neither the received CRC nor closing FLAG are presented to the processor. The processor may drop RxE or leave it active at the end of the received message.

BCP Operation

The operation of the receiver in BCP mode is shown in Figure 5. The receiver initially searches for two successive SYNC characters, of length specified by PCRS₈₋₁₀, that match the contents of PCSAR_L. The next non-SYNC character or next SYNC character if stripping is not specified (PCRSAR₁₃ = 0), causes RxA to be asserted and enables the receiver data path from CCSR through HSR_L to RxSR. All characters following the first non-SYNC are assembled in RxSR and loaded into RDSR_L. RxDa is active when a character is available in RDSR_L. RxSA is active on a 0 to 1 transition of any bit in RDSR_H. The signals are cleared when RDSR_L or RDSR_H are read respectively.

If CRC-16 error control is specified by PCSAR₈₋₁₀, the processor must determine the last character received prior to the CRC field. When that character is loaded into RDSR_L and RxDA is asserted, the received CRC will be in CCSR and HSR_L. To check for a transmission error, the processor must read the receiver status (RDSR_H) and examine RDSR₁₅. This bit will be set for one character time if an error free message has been received. If RDSR₁₅ = 0, the CRC-16 is in error. Note that this bit should be examined only at the end of a message and that the accumulated CRC will include all characters starting with the first non-SYNC character at the start of the message. In particular, SYNC's in the middle of a message, DLE characters, and the first SOH or STX after line turn around are subject to CRC.

If VRC had been selected for error control, parity (odd or even) is regenerated on each character and check with the parity bit received. A discrepancy causes RDSR₁₅ to be set and RxSA to be asserted. This must be sensed by the processor. The received parity bit is stripped before the character is presented to the processor. The processor should compute and check LRC if required.

When the processor has read the last character of the message, it should drop RxE which disables the receiver logic and initializes all receiver registers and timing.

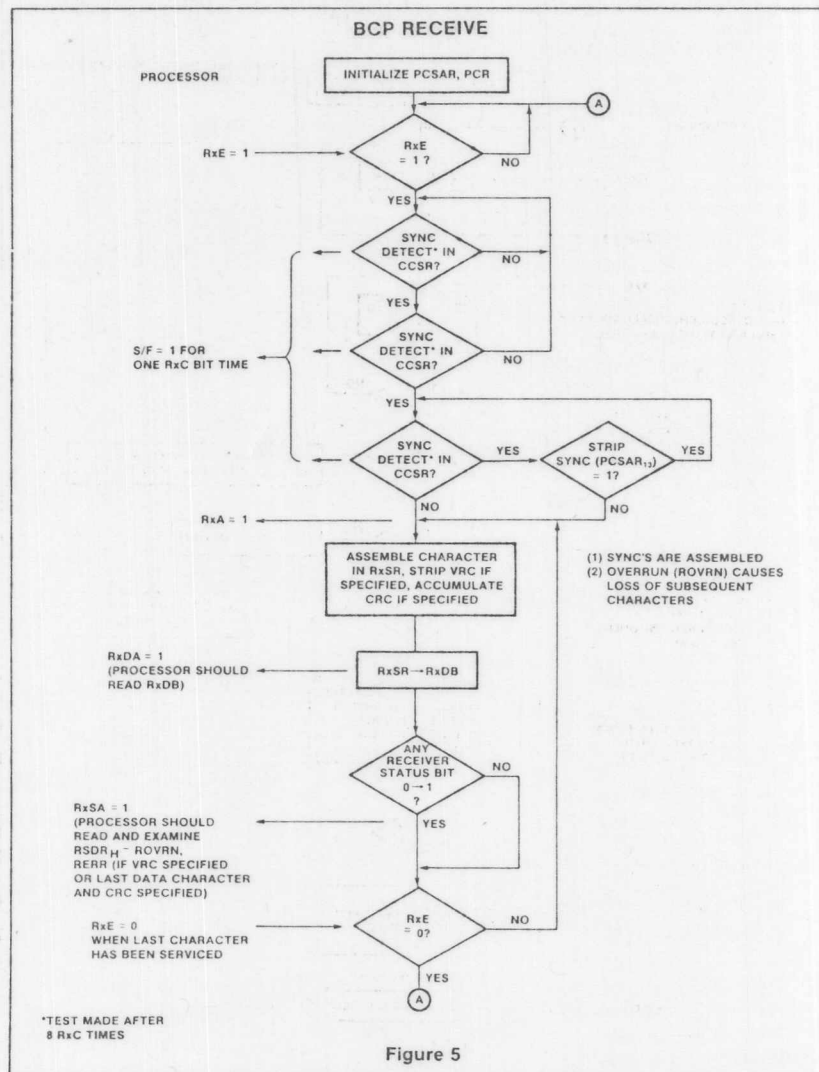


Figure 5

TRANSMITTER OPERATION

General

After the parameter control register (PCSR and PCR) have been initialized, TxE must be set high to enable the transmitter data path. TxSO is held to mark until TSOM (TDSR₀) is set. Then, transmitter operation depends on protocol mode.

BOP Operation

Transmitter operation for BOP is shown in Figure 6. A FLAG is sent when the processor sets the Transmit Start of Message bit (TSOM). The FLAG is used to synchronize the message that follows. TxA will be asserted after TSOM is set. When TxBE is asserted by the MPCC, the processor should load

TDSR_L with the first character of the message. TSOM should be cleared at the same time TDSR_L is loaded (16-bit data bus) or immediately thereafter (8-bit data bus). FLAGs are sent as long as TSOM = 1.

All succeeding characters are loaded into TDSR_L by the processor when TxBE = 1. Each character is serialized in TxSR and transmitted on TxSQ. Internal zero insertion logic stuffs a "0" into the serial bit stream after five successive "1s" are sent. This insures a data character will not match a FLAG, ABORT, or GA reserved control character. As each character is transmitted, the Frame Check Sequence (FCS) is generated as specified by Error Control Mode (PCSA_{R8-10}). The FCS should be the

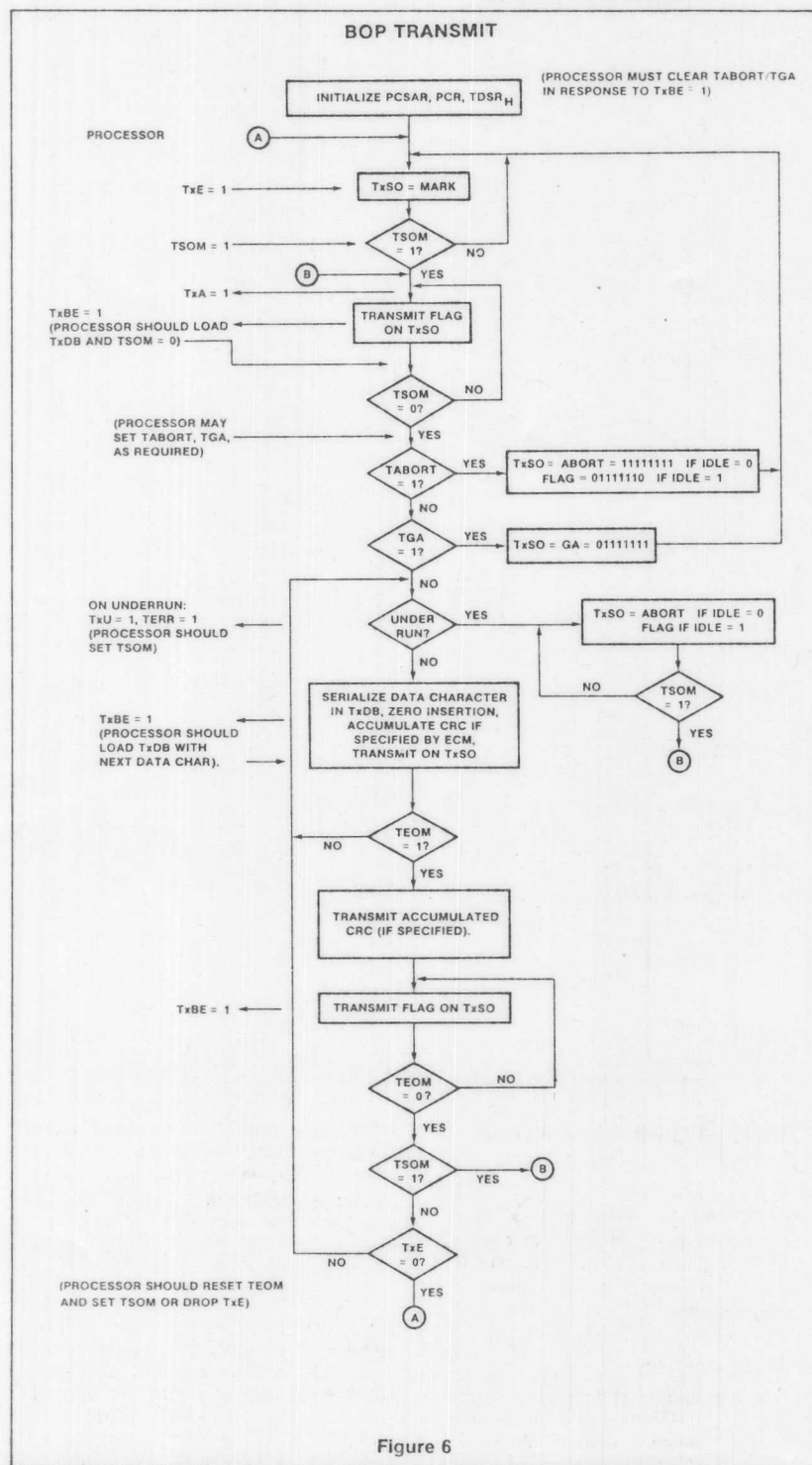


Figure 6

CRC-CCITT polynomial) $X^{16} + X^{12} + X^5 + 1$ preset to 1s. If an underrun occurs (processor is not keeping up with the transmitter), TxU and TERR (TDSR₁₅) will be asserted with ABORT or FLAG used as the TxSO line fill depending on the state of IDLE (PCSAR₁₁). The processor must set TSOM and retransmit the message to recover.

A residual character of 3 to 7 bits may be transmitted at the end of BOP information field to make sure that field is a multiple of 8 bits. In response to TxBE, write the residual character length into TxCL and load TxDB with the residual character. Dynamic alteration of character length should be done in exactly the same sequence.

After the last data character has been loaded into TDSR_L and sent to TxSR (TxBE = 1), the processor should set TEOM (TDSR₉). The MPCC will finish transmitting the last character followed by the FCS and the closing FLAG. The processor should clear TEOM and drop TxE when the next TxBE is asserted. This corresponds to the start of closing FLAG transmission. When TxE has been dropped, TxA will be low 1 1/2 bit times after the last bit of the closing FLAG has been transmitted. TxSO will be marked after the closing FLAG has been transmitted.

If TxE and TEOM are high, the transmitter continues to send FLAGs. The processor may initiate the next message by resetting TEOM and setting TSOM, or by loading TDSR_L with a data character and then simply resetting TEOM (without setting TSOM).

BCP Operation

Transmitter operation for BCP mode is shown in Figure 7. If TxE is high, TxA will be asserted when TSOM = 1. At that time SYNC characters are sent from PCSAR_L or TDSR_L (IDLE = 0 or 1) as long as TSOM = 1. TxBE is asserted at the start of transmission of the first SYNC character. For more than one SYNC, the processor should reassert TSOM in response to the assertion of TxBE. When TSOM = 0 transmission is from TDSR_L, which must be loaded with characters from the processor each time TxBE is asserted. If this loading is delayed for more than one character time, an underrun results: TxU and TERR are asserted and the TxSO line fill depend on IDLE (PCSAR₁₁). The processor must set TSOM and retransmit the message to recover.

CRC-16, if specified by PCSAR₈₋₁₀, is generated on each character transmitted from TDSR_L when TSOM = 0. The processor must set TEOM = 1 after the last data character has been sent to TxSR (TxBE = 1). The MPCC will finish transmitting the last data

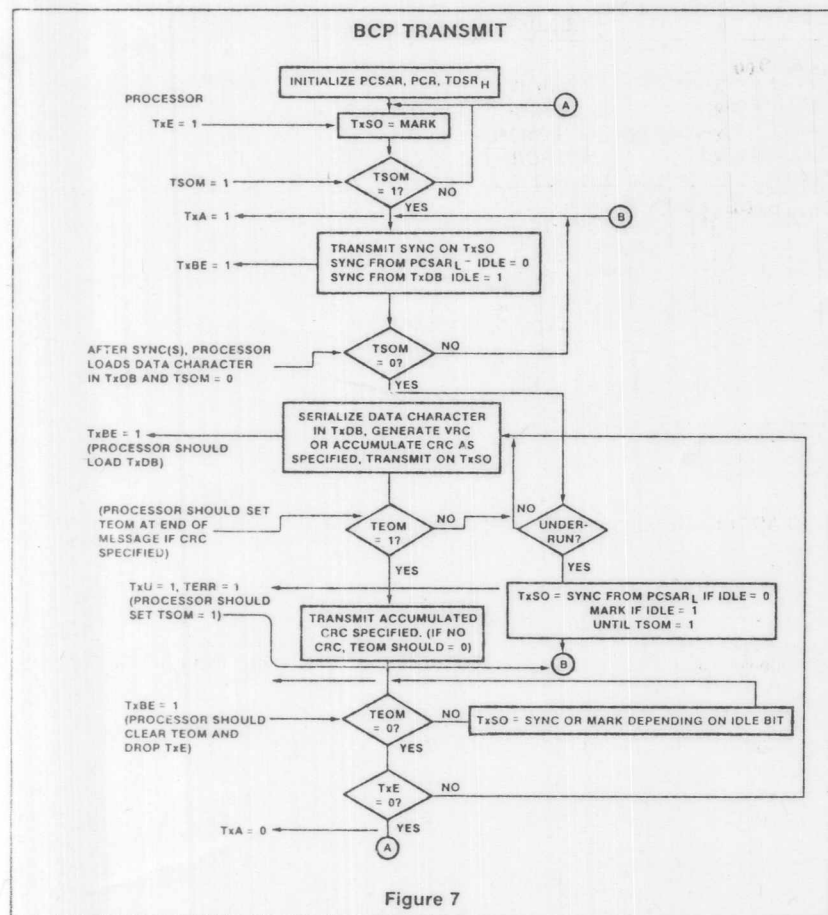


Figure 7

character and the CRC-16 field before sending SYNC characters which are transmitted as long as TEOM = 1. If SYNCs are not desired after CRC-16 transmission, the processor should clear TEOM and lower TxE when the TxBE corresponding to the start of CRC-16 transmission is asserted. When TEOM = 0, the line is marked and a new message may be initiated by setting TxE and TSQM.

If LRC is required, it must be generated by the processor and transmitted after the last data character. TEOM should not be set under this condition. If VRC is specified, it is generated on each data character and the data character length must not exceed 7 bits. For software LRC or CRC TEOM should be set only if SYNCs are required at the end of the message block.

SPECIAL CASE

the capability to transmit 16 spaces is provided for line turnaround in half duplex mode or for a control recovery situation.

This is achieved by setting TSOM and TEOM, clearing TEOM when TxBE = 1, and proceeding as required.

PROGRAMMING

Prior to initiating data transmission or reception, PCSAR and PCR must be loaded with control information from the processor. The contents of these registers (see Register Format section) will configure the MPCC for the user's specific data communication environment. These registers should be loaded during power-on initialization and after a reset operation. They can be changed at any time that the respective transmitter or receiver is disabled.

The default value for all registers is zero. This corresponds to BOP, primary station mode, 8-bit character length, FCS = CRC-CCITT preset to 1s.

For BOP mode the character length register (PCR) may be set to the desired values during system initialization. The address and control fields will automatically be 8-

bits. If a residual character is to be transmitted, TxCL should be changed to the residual character length prior to transmission of that character.

DATA BUS CONTROL

The processor must set up the MPCC register address (A2-A0), chip enable (CE), byte select (BYTE), and read/write ($\bar{R}/W$) inputs before each data bus transfer operation.

During a read operation ($\bar{R}/W = 0$), the leading edge of DBEN will initiate an MPCC read cycle. The addressed register will place its contents on the data bus. If BYTE = 1, the 8-bit byte is placed on DB15-08 or DB07-00 depending on the H/L status of the register addressed. Unused bits in RDSRL are zero. If BYTE = 0, all 16 bits (DB15-00) contain MPCC information. The trailing edge of DBEN will reset RxDA and/or RxSA if RDSRH or RDSRL is addressed respectively.

DBEN acts as the enable and strobe so that the MPCC will not begin its internal read cycle until DBEN is asserted.

During a write operation ($\bar{R}/W = 1$), data must be stable on DB₁₅₋₀₈ and/or DB₀₇₋₀₀ prior to the leading edge of DBEN. The stable data is strobed into the addressed register by DBEN. TxBE will be cleared if the addressed register was TDSRH or TDSRL.

A2	A1	A0	REGISTER
BYTE = 0 16-BIT DATA BUS = DB ₁₅ - DB ₀₀			
0	0	X	RDSR
0	1	X	TDSR
1	0	X	PCSAR
1	1	X	PCR*
BYTE = 1 8-BIT DATA BUS = DB ₇₋₀ or DB ₁₅₋₈ **			
0	0	0	RDSR _L
0	0	1	RDSR _H
0	1	0	TDSR _L
0	1	1	TDSR _H
1	0	0	PCSAR _L
1	0	1	PCSAR _H
1	1	0	PCR _L *
1	1	1	PCR _H

NOTES

* PCR lower byte does not exist. It will be all "0"s when read.

** Corresponding high and low order pins should be tied together.

Table 4 MPCC REGISTER ADDRESSING

BIT	NAME	MODE	FUNCTION																																				
00-07	Not Defined																																						
08-10	RxCL	BOP/BCP	Receiver Character Length is loaded by the processor depending on RxBC when RxCLE = 0. <table> <tr> <th>10</th><th>9</th><th>8</th><th>Char. length (bits)</th></tr> <tr><td>0</td><td>0</td><td>0</td><td>8</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>2</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>3</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>4</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>5</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>6</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>7</td></tr> </table>	10	9	8	Char. length (bits)	0	0	0	8	0	0	1	1	0	1	0	2	0	1	1	3	1	0	0	4	1	0	1	5	1	1	0	6	1	1	1	7
10	9	8	Char. length (bits)																																				
0	0	0	8																																				
0	0	1	1																																				
0	1	0	2																																				
0	1	1	3																																				
1	0	0	4																																				
1	0	1	5																																				
1	1	0	6																																				
1	1	1	7																																				
11	RxCLE	BOP/BCP	Receiver Character Length Enable should be zero when the processor loads RxCL. The remaining bits of PCR are not affected during loading.																																				
12	TxCLE	BOP/BCP	Transmitter Character Length Enable should be zero when the processor loads TxCL. The remaining bits of PCR are not affected during loading.																																				
13-15	TxCL	BOP/BCP	Transmitter Character Length is loaded by the processor when TxCLE = 0. Character bit length specification format is identical to RxCL.																																				

Table 5 PARAMETER CONTROL REGISTER (PCR)-(R/W)

BIT	NAME	MODE	FUNCTION																																																						
00-07	S/AR	BOP BCP	SYNC/ADDRESS Register. Contains the secondary station address if the MPCC is a secondary station. The contents of this register is compared with the first received non-FLAG character to determine if the message is meant for this station. SYNC character is loaded into this register by the processor. It is used for receive and transmit bit synchronization with bit length specified by RxCL and TxCL.																																																						
08-10	ECM	BOP/BCP	<table><tr><th>Error Control Mode</th><th>10</th><th>9</th><th>8</th><th>Mode</th><th>Char. length</th></tr><tr><td>CRC-CCITT preset to 1's</td><td>0</td><td>0</td><td>0</td><td>BOP</td><td>1-8</td></tr><tr><td>CRC-CCITT preset to 0's</td><td>0</td><td>0</td><td>1</td><td>BOP</td><td>1-8</td></tr><tr><td>Not used</td><td>0</td><td>1</td><td>0</td><td>---</td><td></td></tr><tr><td>CRC-16 preset to 0's</td><td>0</td><td>1</td><td>1</td><td>BCP</td><td>8</td></tr><tr><td>VRC odd</td><td>1</td><td>0</td><td>0</td><td>BCP</td><td>5-7</td></tr><tr><td>VRC even</td><td>1</td><td>0</td><td>1</td><td>BCP</td><td>5-7</td></tr><tr><td>Not used</td><td>1</td><td>1</td><td>0</td><td>---</td><td></td></tr><tr><td>No error control</td><td>1</td><td>1</td><td>1</td><td>BCP</td><td>5-8</td></tr></table> ECM should be loaded by the processor during initialization or when both data paths are idle.	Error Control Mode	10	9	8	Mode	Char. length	CRC-CCITT preset to 1's	0	0	0	BOP	1-8	CRC-CCITT preset to 0's	0	0	1	BOP	1-8	Not used	0	1	0	---		CRC-16 preset to 0's	0	1	1	BCP	8	VRC odd	1	0	0	BCP	5-7	VRC even	1	0	1	BCP	5-7	Not used	1	1	0	---		No error control	1	1	1	BCP	5-8
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Not used	1	1	0	---																																																					
No error control	1	1	1	BCP	5-8																																																				
11	IDLE		Determines line fill character to be used if transmitter underrun occurs (TxU asserted and TERR set) and transmission of special characters for BOP/BCP.																																																						
		BOP BCP	IDLE = 0, transmit ABORT characters during underrun and when TABORT = 1. IDLE = 1, transmit FLAG characters during underrun and when TABORT = 1. IDLE = 0 transmit initial SYNC characters and underrun line fill characters from the S/AR. IDLE = 1 transmit initial SYNC characters from TxDB and marks TxSO during underrun.																																																						
12	SAM	BOP	Secondary Address Mode = 1 if the MPCC is a secondary station. This facilitates automatic recognition of the received secondary station address. When transmitting, the processor must load the secondary address into TxDB. SAM = 0 inhibits the received secondary address comparison which serves to activate the receiver after the first non-FLAG character has been received.																																																						
13	SS/GA	BOP BCP	Strip SYNC/Go Ahead. Operation depends on mode. For loop mode only, SS/GA = 1 permits GA character to terminate a received message. When a GA is detected REOM and RAB/GA will be set and the processor should terminate the repeater function. SS/GA = 0 permits only a FLAG or ABORT character to terminate a message. SS/GA = 1, causes the receiver to strip SYNC's immediately following the first two SYNC's detected. SYNC's in the middle of a message will not be stripped. SS/GA = 0, presents any SYNC's after the initial two SYNC's to the processor.																																																						
14	PROTO	BOP BCP	Determines MPCC Protocol mode PROTO = 0 BOP PROTO = 1 BCP																																																						
15	APA	BOP	All Parties Address. If this bit is set, the receiver data path is enabled by an address field of '11111111' as well as the normal secondary station address.																																																						

Table 6 PARAMETER CONTROL SYNC/ADDRESS REGISTER (PCSAR)-(R/W)

BIT	NAME	MODE	FUNCTION
00-07	TxDB	BOP/BCP	Transmit Data Buffer. Contains processor loaded characters to be serialized in TxSR and transmitted on TxSO.
08	TSOM	BOP BCP	Transmitter Start of Message. Set by the processor to initiate message transmission provided TxE = 1. TSOM = 1 generates FLAGs. When TSOM = 0 transmission is from TxDB and FCS generation begins. FCS, as specified by PCSAR₈₋₁₀, should be CRC-CCITT preset to 1's. TSOM = 1 generates SYNCs from PCSAR_L or transmits from TxDB for IDLE = 0 or 1 respectively. When TSOM = 0 transmission is from TxDB and CRC generation (if specified) begins.

Table 7 TRANSMIT DATA/STATUS REGISTER (TDSR) (R/W except TDSR 15)

BIT	NAME	MODE	FUNCTION
09	TEOM	BOP	Transmit End of Message. Used to terminate a transmitted message when CRC error checking is used. TEOM = 1 causes the FCS and the closing FLAG to be transmitted following the transmission of the data character in TxSR. FLAGs are transmitted until TEOM = 0. ABORT or GA are transmitted if TABORT or TGA are set when TEOM = 1.
		BCP	TEOM = 1 causes CRC-16 to be transmitted (if selected) followed by SYNCs from PCSAR _L or TxDB (IDLE = 0 or 1). Clearing TEOM prior to the end of CRC-16 transmission (when TxBE = 1) causes TxSO to be marked following the CRC-16. TxE must be dropped before a new message can be initiated. If CRC is not selected, TEOM should not be set.
10	TABORT	BOP	Transmitter Abort = 1 will cause ABORT or FLAG to be sent (IDLE = 0 or 1) after the current character is transmitted. (ABORT = 11111111)
11	TGA	BOP	Transmit Go Ahead (GA) instead of FLAG when TEOM = 1. This facilitates repeater termination in loop mode. (GA = 01111111)
12-14	Not Defined		
15	TERR	Read only BOP BCP	Transmitter Error = 1 indicates the TxDB has not been loaded in time to maintain continuous transmission. TxU will be asserted to inform the processor of this condition. TERR is cleared by setting TSOM. ABORT's or FLAG's are sent as fill characters (IDLE = 0 or 1) SYNC's or MARK's are sent as fill characters (IDLE = 0 or 1). For IDLE = 1 the last character before underrun is not valid.

Table 7 TRANSMIT DATA/STATUS REGISTER (TDSR) (R/W except TDSR 15) (Cont'd)

BIT	NAME	MODE	FUNCTION
00-07	RxDB	BOP/BCP	Receiver Data Buffer. Contains assembled characters from the RxSR. If VRC is specified, the parity bit is stripped.
08	RSOM	BOP	Receiver Start of Message = 1 when a FLAG followed by a non-FLAG has been received and the latter character matches the secondary station address if SAM = 1. RxA will be asserted when RSOM = 1. RSOM resets itself after one character time and has no effect on RxSA.
09	REOM	BOP	Receiver End of Message = 1 when the closing FLAG is detected and the last data character is loaded into RxDB or when an ABORT/GA character is received. REOM is cleared on reading RDSRH, reset operation, or dropping of RxE.
10	RAB/GA	BOP	Received ABORT or GA character = 1 when the receiver senses an ABORT character if SS/GA = 0 or a GA character if SS/GA = 1. RAB/GA is cleared on reading RDSRH, reset operation, or dropping of RxE. A received ABORT inhibits RxDA.
11	ROR	BOP/BCP	Receiver Overrun = 1 indicates the processor has not read the last character in the RxDB within one character time. Subsequent characters will be lost. ROR is cleared on reading RDSRH, reset operation, or dropping of RxE.
12-14	ABC	BOP	Assembled Bit Count. Specifies the number of bits in the last received data character of a message and should be examined by the processor when REOM = 1 (RxDA and RxSA asserted). ABC = 0 indicates the message was terminated (by a FLAG or GA) on a character boundary as specified by PCSCR ₈₋₁₀ . Otherwise, ABC = number of bits in the last data character. ABC is cleared when RDSRH is read, reset operation, or dropping RxE. The residual character is right justified in RDSRL.
15	RERR	BOP BCP	Receiver Error indicator should be examined by the processor when REOM = 1 in BOP, or when the processor determines the last data character of the message in BCP with CRC or when RxSA is set in BCP with VRC. CRC-CCITT preset to 1's should be specified by PCSAR ₈₋₁₀ : RERR = 1 indicates FCS error (CRC ≠ F0B8) RERR = 0 indicates FCS received correctly (CRC = F0B8) CRC-16 preset to 0's on 8-bit data characters specified by PCSAR ₈₋₁₀ : RERR = 1 indicates CRC-16 received correctly (CRC=0). RERR = 0 indicates CRC-16 error (CRC ≠ 0) VRC specified by PCSAR ₈₋₁₀ : RERR = 1 indicates VRC error RERR = 0 indicates VRC is correct

Table 8 RECEIVER DATA/STATUS REGISTER (RDSR)-(Read Only)

ABSOLUTE MAXIMUM RATINGS¹

PARAMETER		RATING	UNIT
T _A	Operating ambient temperature ²	0 to +70	°C
T _{STG}	Storage temperature	-65 to +150	°C
V _{CC}	Input or output voltages with respect to GND ³	-0.3 to +15	V
	With respect to GND	-0.3 to +7	V

DC ELECTRICAL CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = +5V ±5%^{4,5,6}

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V _{IL}	Input voltage Low				0.8	V
V _{IH}	Input voltage High		2.0			
V _{OL}	Output voltage Low				0.4	V
V _{OH}	Output voltage High	I _{OL} = 1.6mA I _{OH} = -100μA	2.4			
I _{CC}	Power supply current	V _{CC} = 5.25V, T _A = 0°C			150	mA
I _{IL}	Leakage current Input	V _{IN} = 0 to 5.25V			10	μA
I _{OL}	Leakage current Output	V _{OUT} = 0 to 5.25V			10	μA
C _{IN}	Capacitance Input	V _{IN} = 0V, f = 1MHz			20	pF
C _{OUT}	Capacitance Output	V _{OUT} = 0V, f = 1MHz			20	pF

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5V ± 5%, AC timing indicated is with outputs unloaded.^{4,5,6}

PARAMETER		LIMITS			UNIT
		Min	Typ	Max	
t _{ACS}	Setup and hold time Address/control setup	50			ns
t _{ACH}	Address/control hold	0			
t _{DS}	Data bus setup (write)	50			
t _{DH}	Data bus hold (write)	0			
t _{RXS}	Receiver serial data transfer	150			
t _{RxH}	Receive serial data hold	150			
t _{RES}	Pulse width RESET	250			ns
t _{DBEN}	Pulse width DBEN	250			
t _{DD}	Delay time Data bus (read)			200	ns
t _{TxD}	Transmit serial data			300	
t _{DF}	Data bus float time (read)			150	ns
f	Clock (RxC, TxC) frequency			500	kHz
t _{CLK1}	Clock high	1000			ns
t _{CLK0}	Clock low	1000			ns

PRELIMINARY SPECIFICATION

2652

NOTES

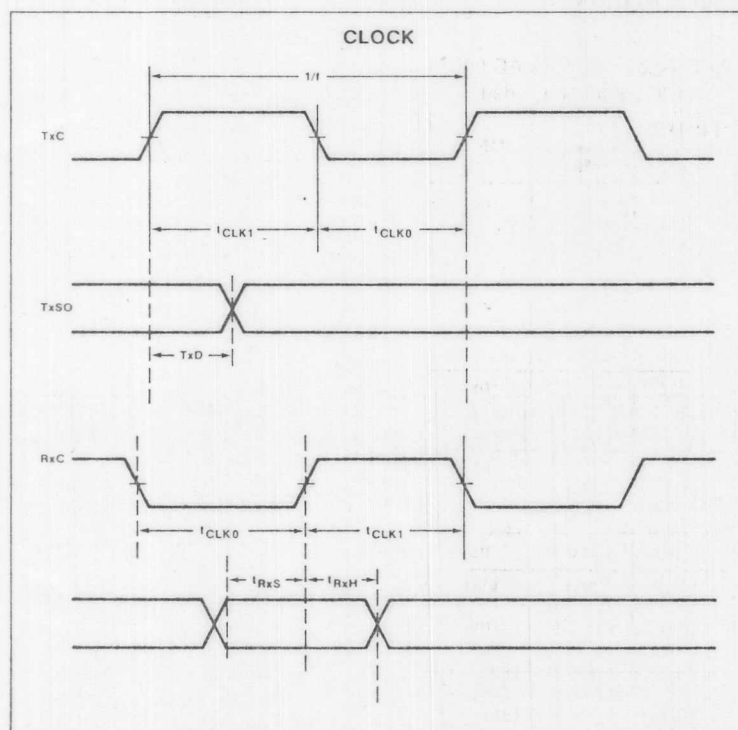
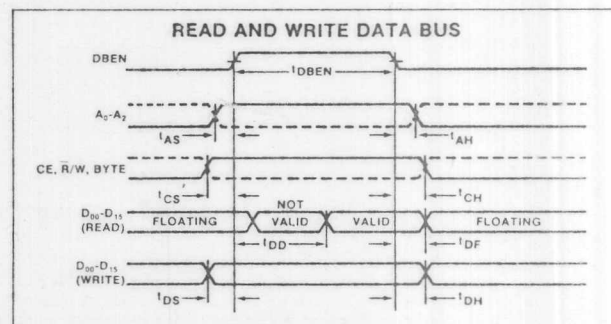
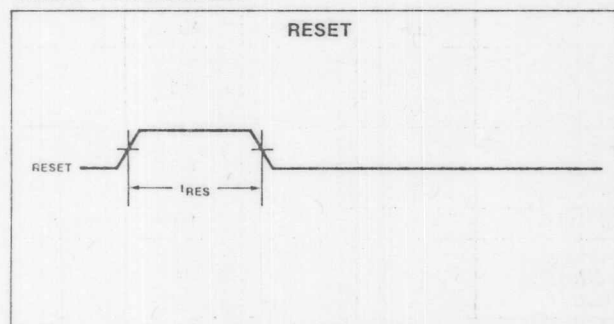
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operation sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on +150°C maximum junction temperature and thermal resistance of 60°C/W junction to ambient (IQ ceramic package).
3. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.

4. Parameters are valid over operating temperature range unless otherwise specified.
5. All voltage measurements are referenced to ground. All time measurements are at V_{OH} , V_{OL} , V_{IH} , or V_{IL} levels as appropriate.
6. Typical values are at +25°C, nominal supply voltages, and nominal process parameters.

PRELIMINARY SPECIFICATION

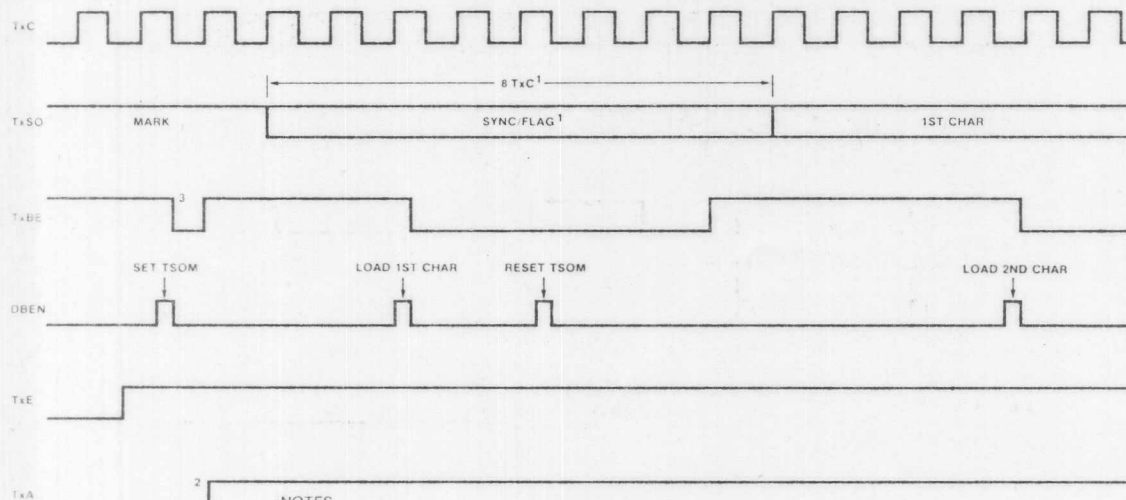
Manufacturer reserves the right to make design and process changes and improvements.

TIMING DIAGRAMS



TIMING DIAGRAMS (Cont'd)

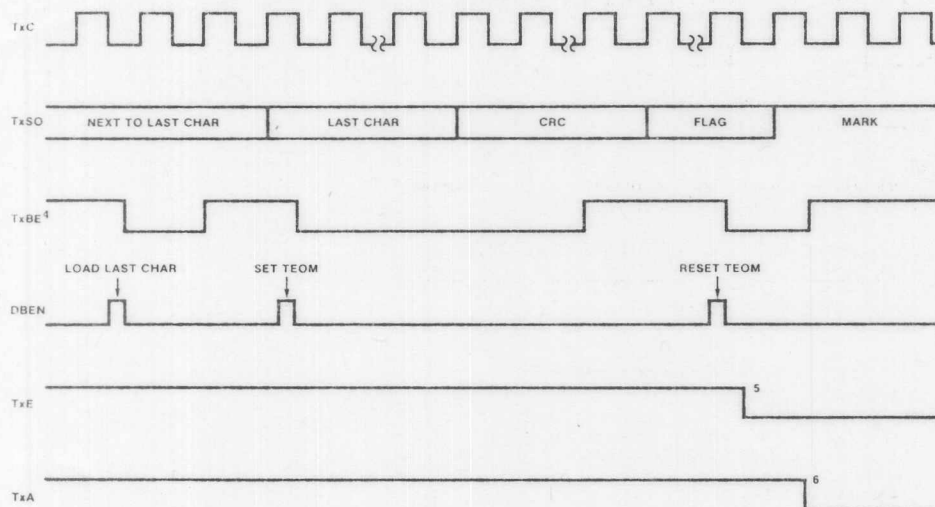
TRANSMIT—START OF MESSAGE



NOTES

1. SYNC may be 5 to 8 bits and will contain parity bit as specified.
2. TxA goes high relative to TxC rising edge after TxE has been raised and TSOM has been set.
3. TxBE goes low relative to DBEN falling edge on the first write transfer into TSDR after TxE has been raised. It is reasserted 1 TxC time before the first bit of the transmitted SYNC/FLAG. TxBE then goes low relative to DBEN falling edge when writing into TDSRH and/or TDSRL. It is reasserted on the rising edge of the TxC that corresponds to the transmission of the last bit of each character, except in BOP mode when the CRC is to be sent as the next character (see Transmit Timing-End of Message).

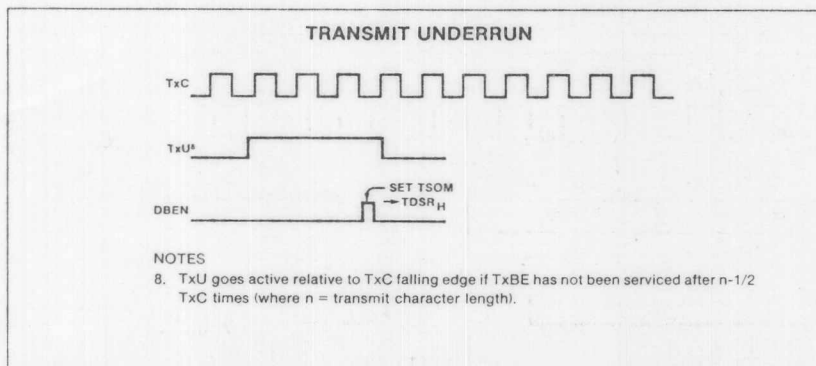
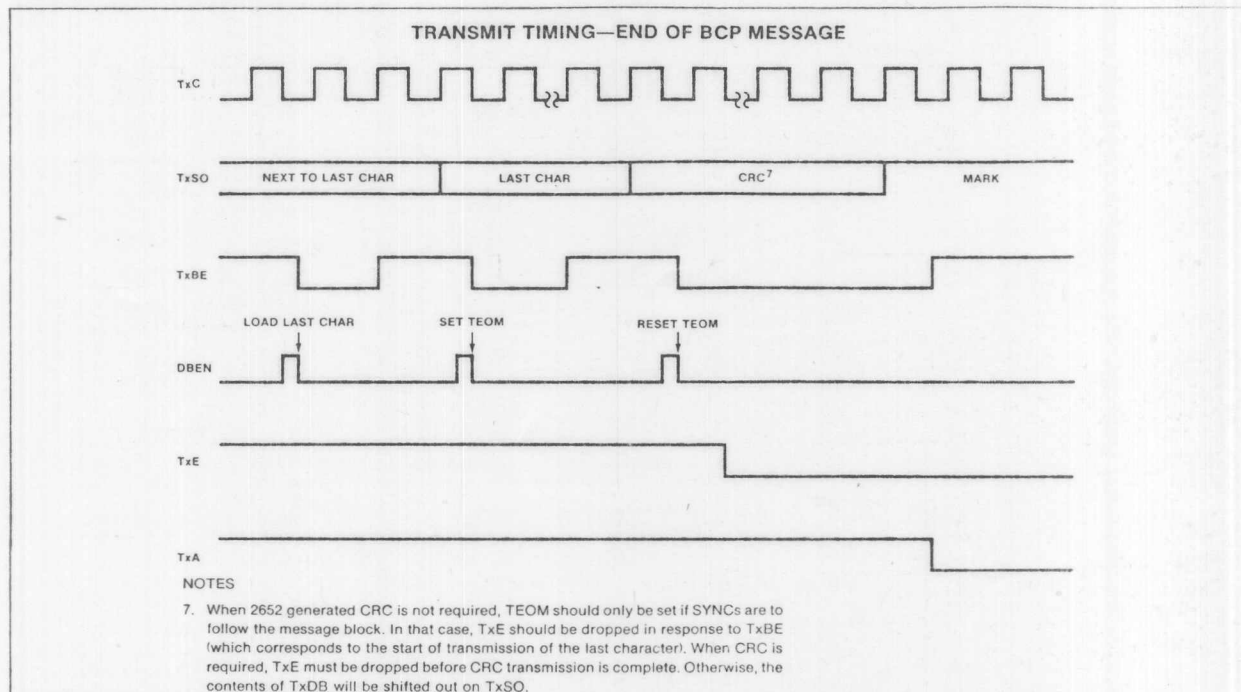
TRANSMIT—END OF BOP MESSAGE



NOTES

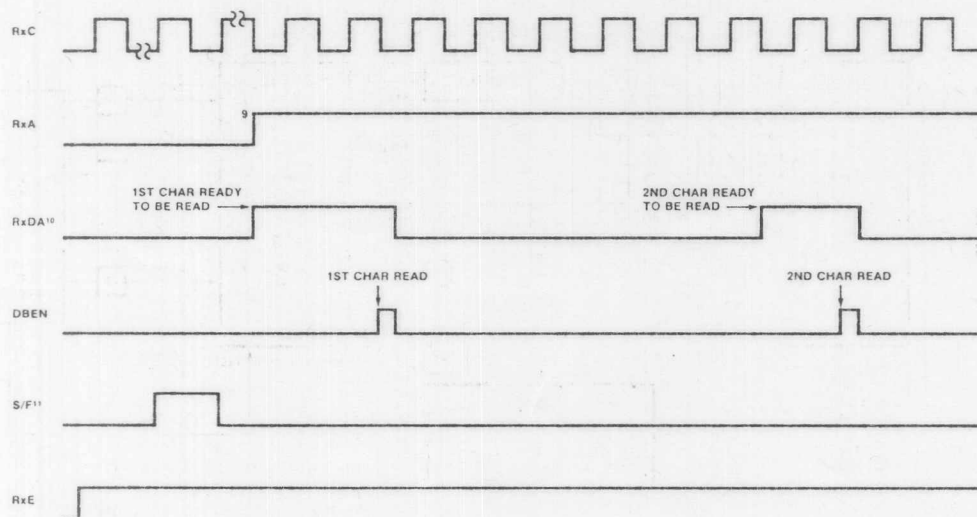
4. TxBE goes low relative to the falling edge of DBEN corresponding to loading TDSRH/L. It goes high one TxC before character transmission begins and also when TxA has been dropped.
5. TxE can be dropped before resetting TEOM if TxBE (corresponding to the closing FLAG) is high. Alternatively TxE can remain high and a new message initiated.
6. TxA goes low after TxE has been dropped and 1 1/2 TxC's after the last bit of the closing FLAG has been transmitted.

TIMING DIAGRAMS (Cont'd)



TIMING DIAGRAMS (Cont'd)

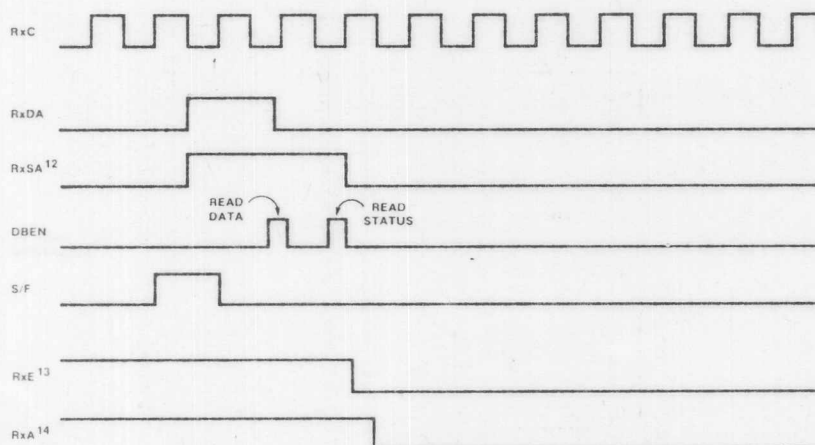
RECEIVE—START OF MESSAGE



NOTES

9. Rx A goes high relative to falling edge of Rx C when Rx E is high and:
 - a. A data character following two SYNC's is in RxDB (BCP mode)
 - b. Character following FLAG is in RxDB (BOP primary station mode)
 - c. Character following FLAG is in RxDB and character matches the secondary station address or All Parties Address (BOP secondary station mode).
10. Rx DA goes high when a character in RxDB is ready to be read. It goes low on the falling edge of DBEN when RxDB is read.
11. S/F goes high relative to rising edge of Rx C anytime a SYNC (BCP) or FLAG (BOP) is detected.

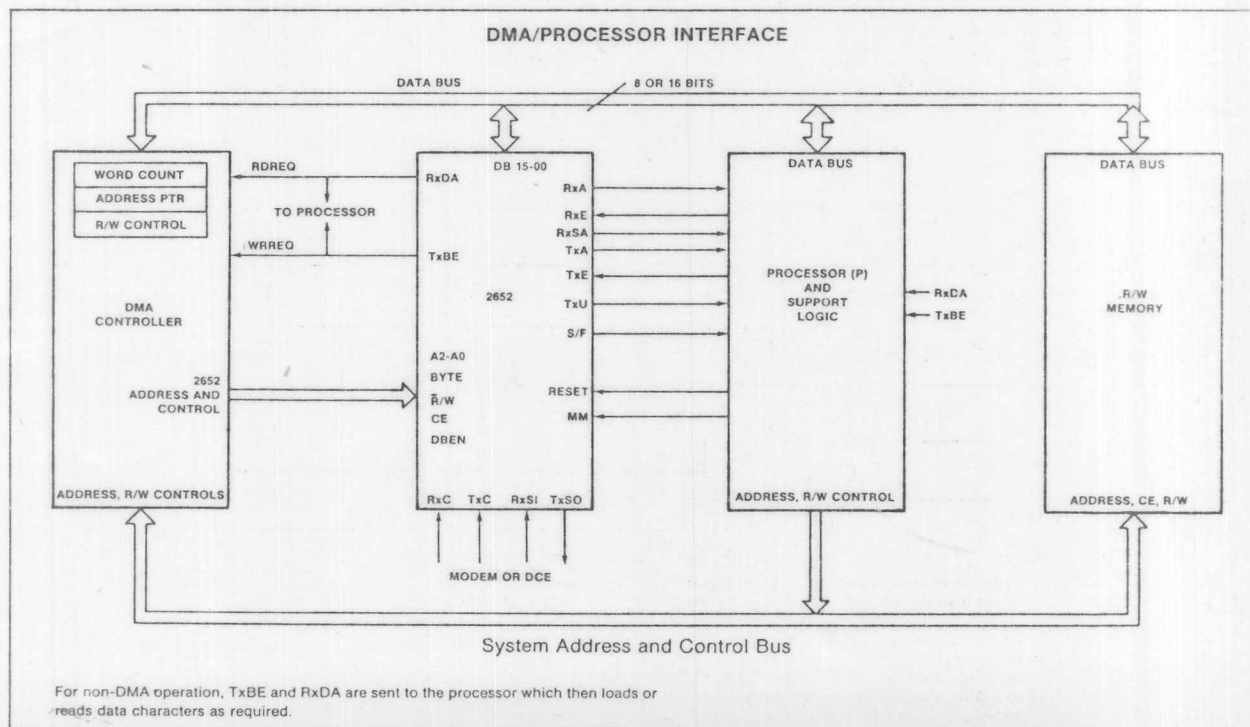
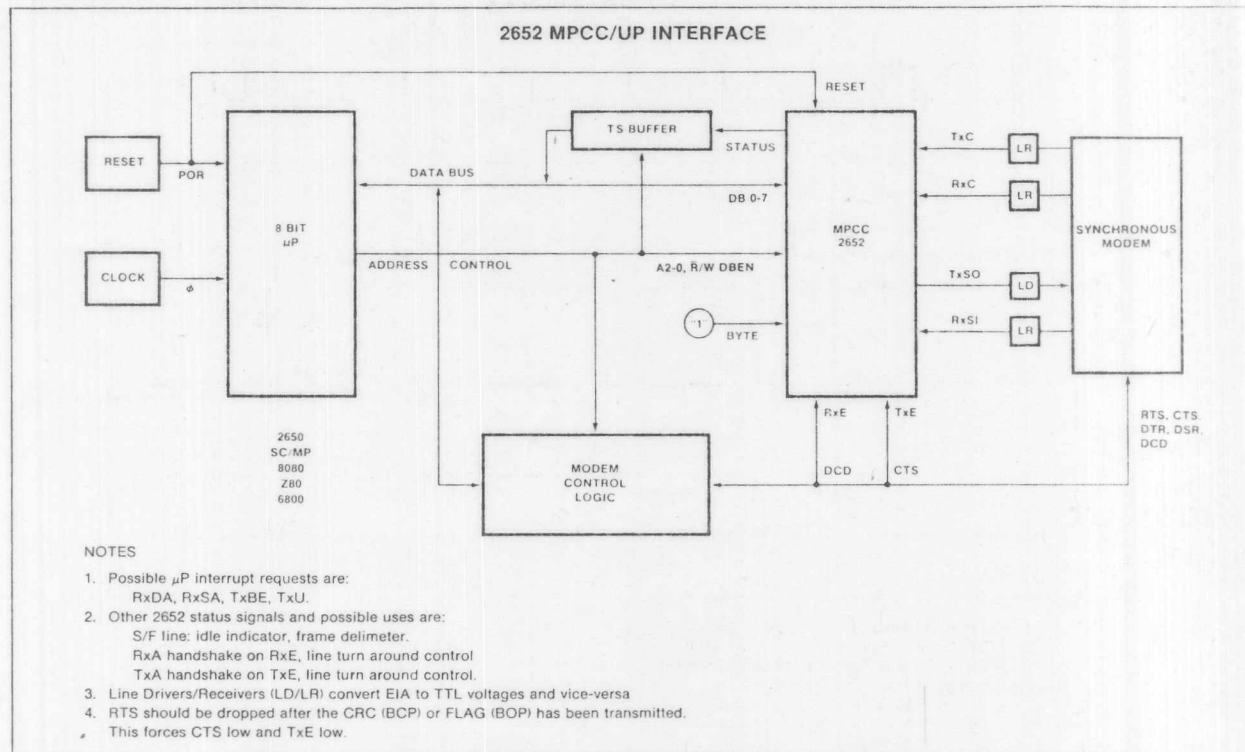
RECEIVE END OF MESSAGE



NOTES

12. At the end of a BOP message, Rx SA goes high when FLAG detection (S/F = 1) forces REOM to be set. Processor should read the last data character (RDSRL) and status (RDSRH) which resets Rx DA and Rx SA respectively. For BCP end of message, Rx SA may not be set. The processor should read the last data character and the status.
13. Rx E must be dropped for BCP but may be left on at the end of a BOP message (see BOP Receive Operation).
14. Rx A is reset relative to the falling edge of Rx C after the closing FLAG of a BOP message; or when Rx E is dropped.

TYPICAL APPLICATIONS



TYPICAL APPLICATIONS (Cont'd)

